EE105 – Fall 2015
Microelectronic Devices and Circuits

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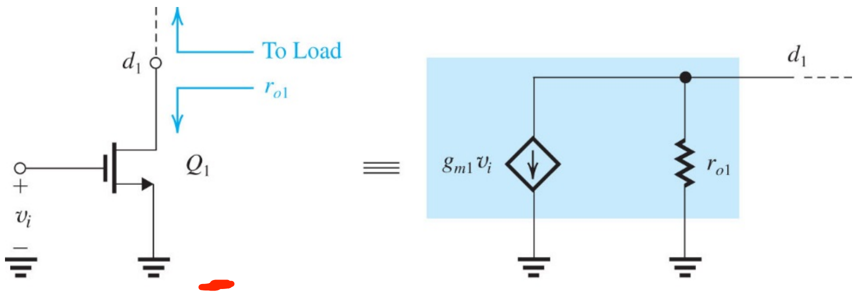
How To Increase Voltage Gain?



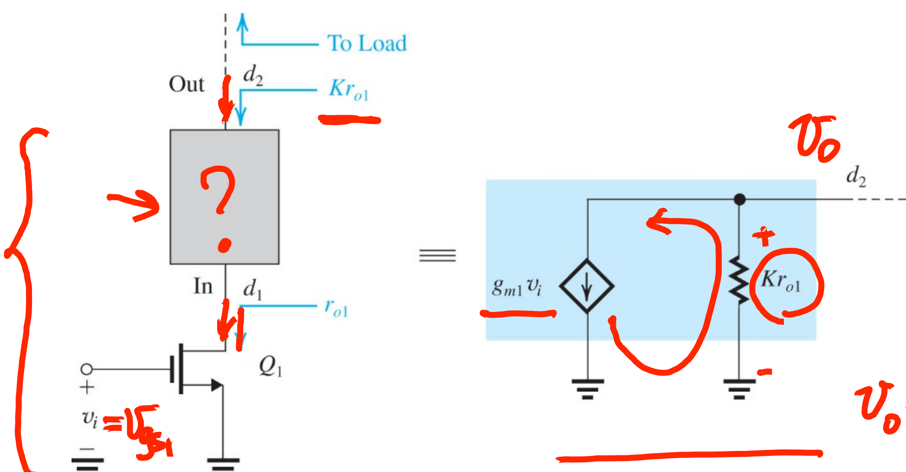
(a)

Voltage gain

∞

$$\left|A_v\right| = g_{m1}\left(r_{o1} \parallel R_L\right) \leq g_{m1}r_{o1}$$

limited by r_{o1}



(b)

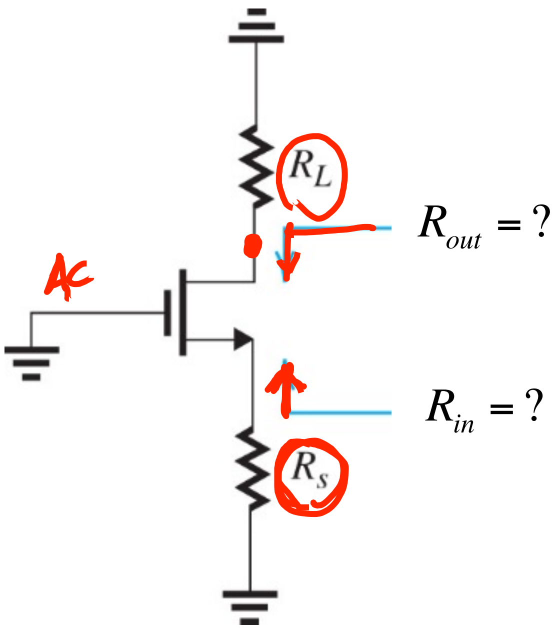
If we can boost up r_{o1} by a factor of K

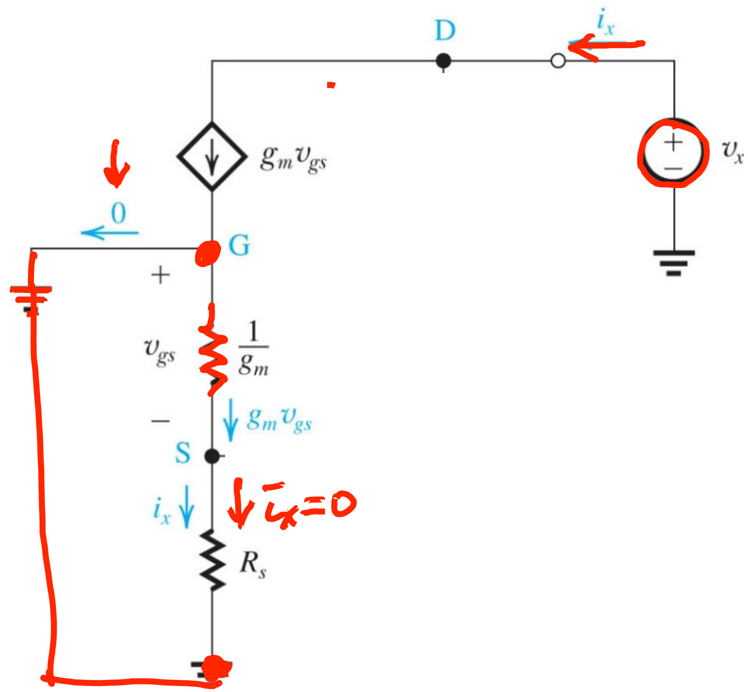
$$\left|A_{v,\max}\right| = g_{m1}Kr_{o1}$$

$v_o = -g_{m1} v_i K r_{o1}$

$A_v = \frac{v_o}{v_i} = -g_{m1} K r_{o1}$

Common Gate Amplifier is an Impedance Transformer





Using T-model

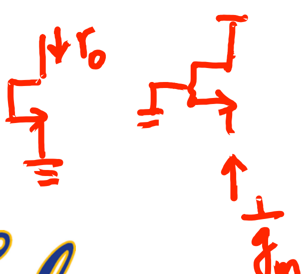
If we don't consider r_o :

$i_x = 0$ since G is grounded

$$R_{out} = \frac{v_x}{i_x} = \infty$$

To find R_{out}

we have to include r_o



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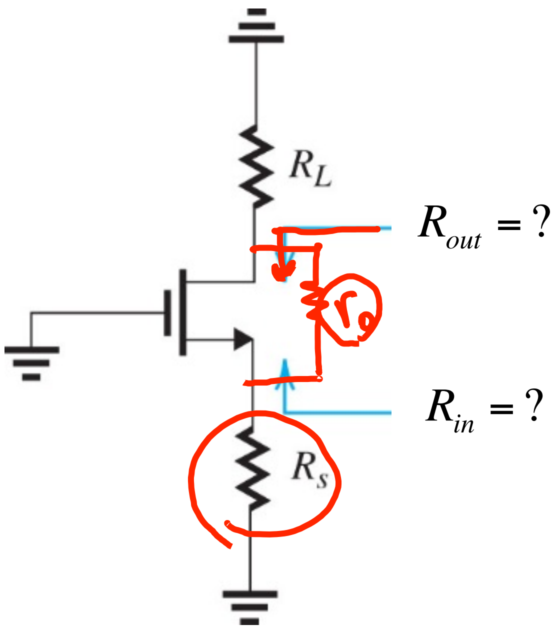
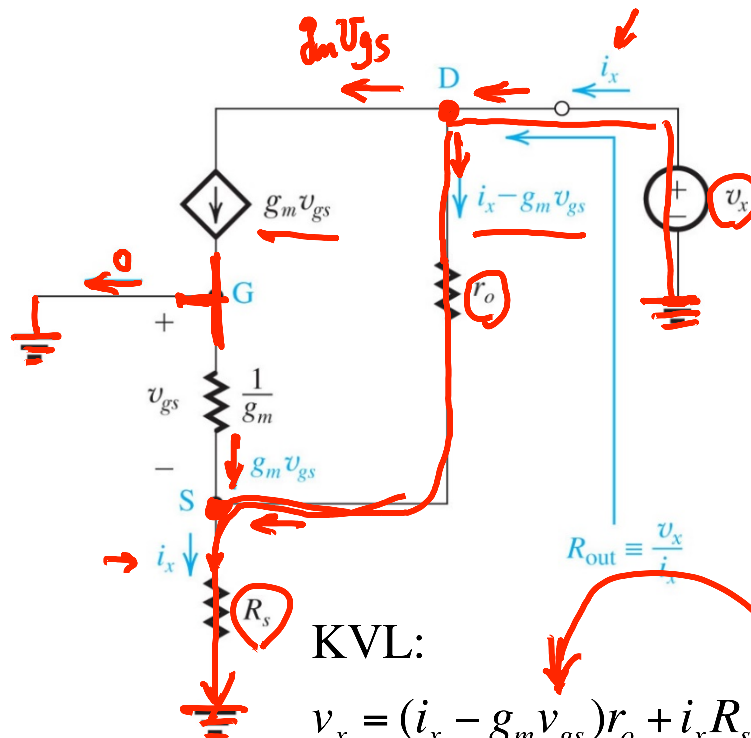




KVL:

$$v_x = (i_x - g_m v_{gs}) r_o + i_x R_s$$

$$v_{gs} = 0 - v_s = -i_x R_s$$

$$v_x = (i_x + g_m i_x R_s) r_o + i_x R_s$$

$$R_{out} = \frac{v_x}{i_x} = r_o + R_s + g_m r_o R_s$$

$$= r_o + (\cancel{1} + g_m r_o) R_s \approx r_o + (g_m r_o) R_s$$

$v_{gs} = v_g - v_s$

$\shortparallel$

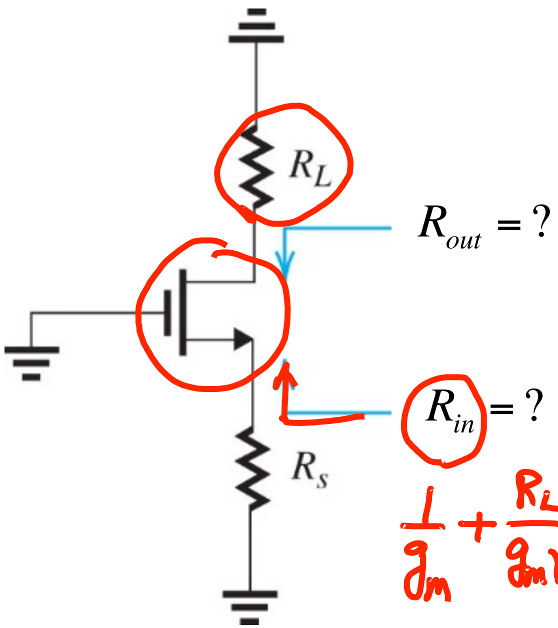
0

$v_s = i_x R_s$

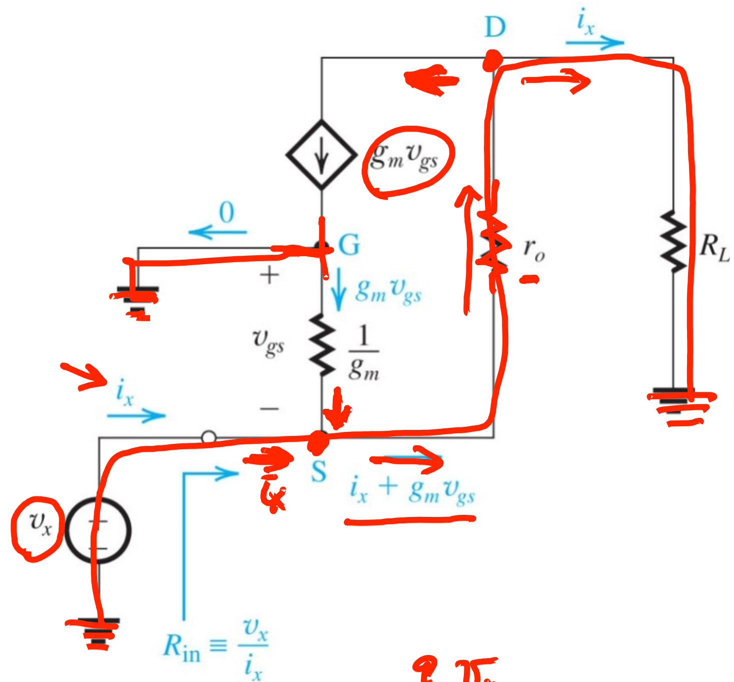
$g_m r_o \gg 1$

~ 100

Common Gate Amplifier is an Impedance Transformer



$\frac{1}{g_m} + \frac{R_L}{g_m r_o}$



$-g_m v_x$

KVL: $v_x = (i_x + g_m v_{gs}) r_o + i_x R_L$

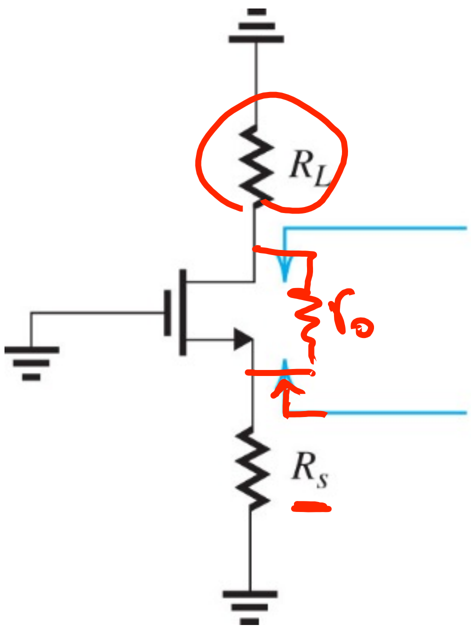
$v_{gs} = 0 - v_s = -v_x$

$(1 + g_m r_o) v_x = (r_o + R_L) i_x$

$$R_{in} = \frac{v_x}{i_x} = \frac{\cancel{r_o} + R_L}{\cancel{1} + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

$g_m r_o \gg 1$

Impedance Transformation of Common Gate Amplifier



$$R_{out} = r_o + R_s + g_m r_o R_s$$
$$\simeq r_o + (g_m r_o) R_s$$

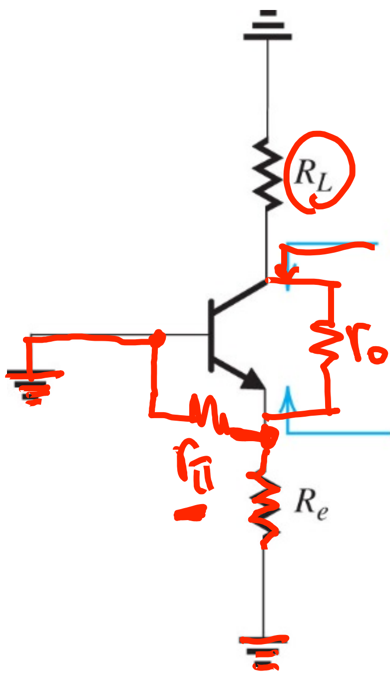
$$R_{in} = \frac{r_o + R_L}{1 + g_m r_o}$$
$$\simeq \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

Impedance transformation:

Look into Drain : R_s amplified by $(g_m r_o)$

Look into Source : R_L reduced by $(g_m r_o)$

Impedance Transformation of Common Base Amplifier



$$R_{\text{out}} = r_o + (R_e \| r_\pi) + g_m r_o (R_e \| r_\pi)$$
$$\simeq r_o + (g_m r_o)(R_e \| r_\pi)$$

$$R_{\text{in}} \simeq r_e \frac{r_o + R_L}{r_o + \frac{R_L}{\beta + 1}}$$
$$\simeq r_e + \frac{R_L}{g_m r_o}, \text{ for } R_L \ll \beta r_o$$

$r_e = \frac{1}{g_m}$

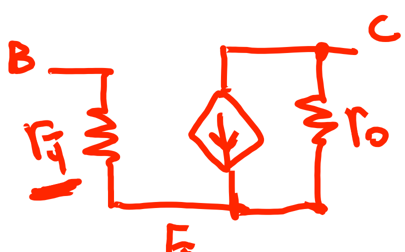
Similar impedance transformati on in Common-Base BJT:

Look into Collector : $R_e \| r_\pi$ amplified by $(g_m r_o)$

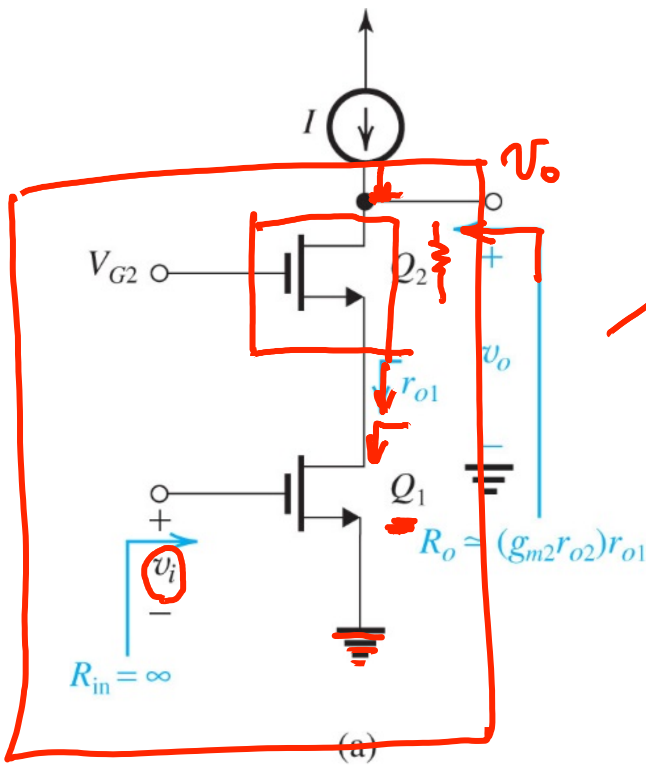
Look into Source : R_L reduced by $(g_m r_o)$

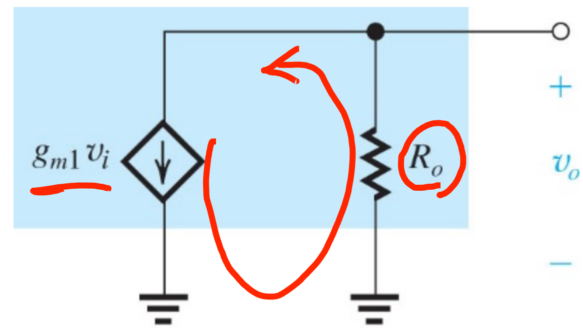
Note R_s in MOS is replaced by $R_e \| r_\pi$ in BJT

Note: for $\beta = \infty$, these formulas reduce to those for the MOSFET



MOS Cascode Amplifier





$$R_o = \cancel{r_{o2}} + \overbrace{(g_{m2}r_{o2})}^{K}r_{o1} \approx \overbrace{(g_{m2}r_{o2})r_{o1}}^{\sim 100}$$

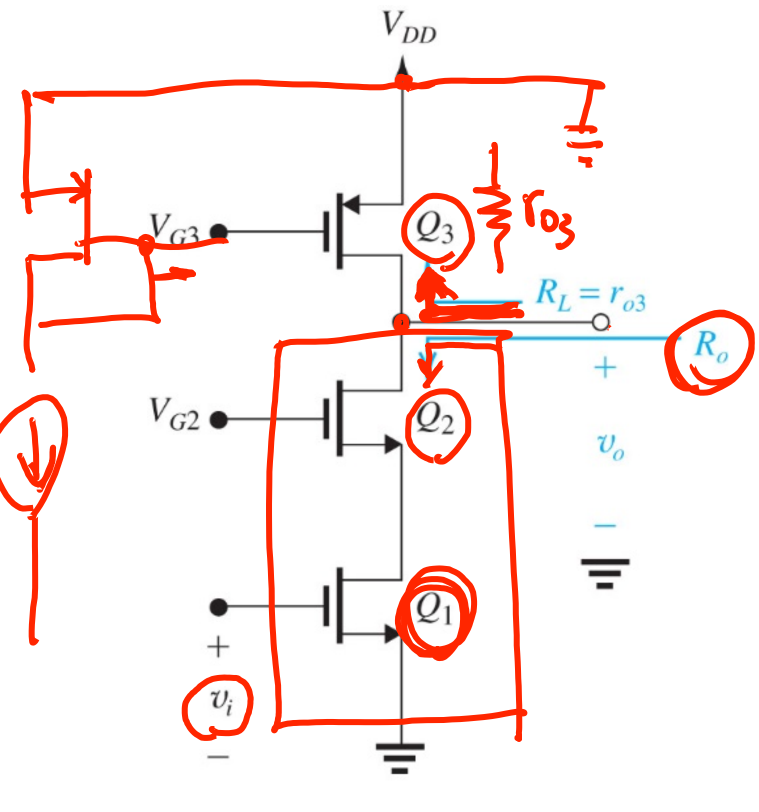
$$A_{vo} = -g_{m1}R_o = -g_{m1}(g_{m2}r_{o2})r_{o1}$$

$$A_{vo} = -(g_{m1}r_{o1})(g_{m2}r_{o2})$$

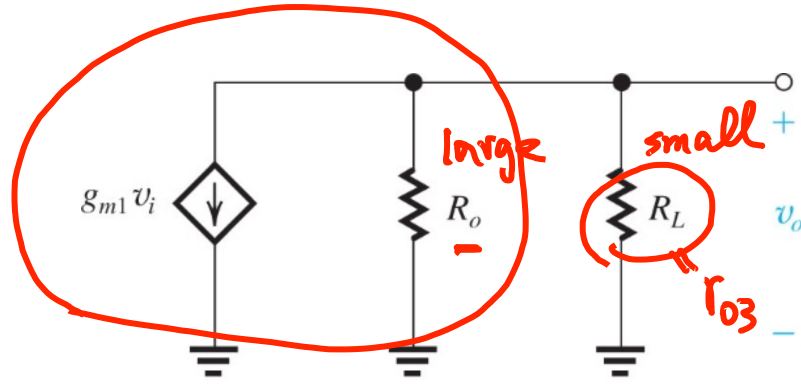
Voltage gain is much higher than single-stage common source (CS) amplifier.

The gain of cascode is almost the square of that of CS

Cascode Amplifier with Simple Active Load



(a)



(b)

$$A_v = -g_{m1}(R_o \parallel R_L)$$

$$R_o \approx (g_{m2} r_{o2}) r_{o1}$$

$$R_L = r_{o3} << R_o$$

$$A_v = -g_{m1} r_{o3}$$

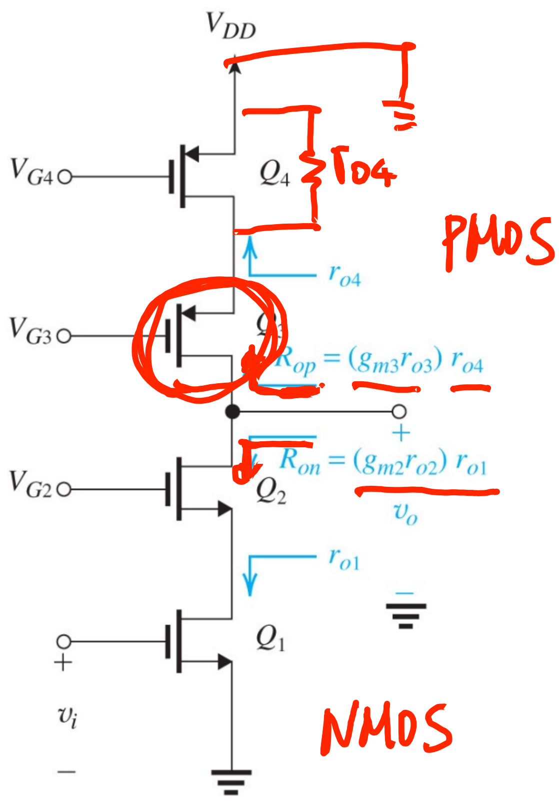
Similar gain as CS amplifier.

No gain boosting.

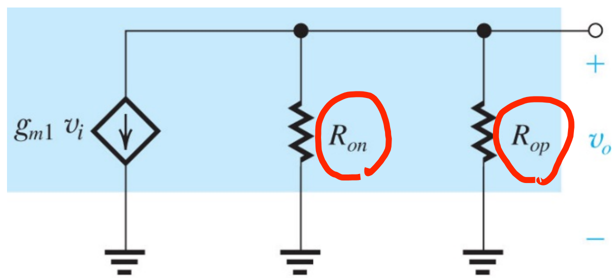
r_o

$R_o = r_{o1} \cdot 100 \gg r_{o3} = R_L$

Cascode Amplifier with Cascode Current-Source Load



(a)



(b)

$$A_v = -g_{m1}(R_{on} \parallel R_{op})$$

$$R_{on} \approx (g_{m2}r_{o2})r_{o1}$$

$$R_{op} \approx (g_{m3}r_{o3})r_{o4}$$

$\Big\} \; \frac{1}{2}$

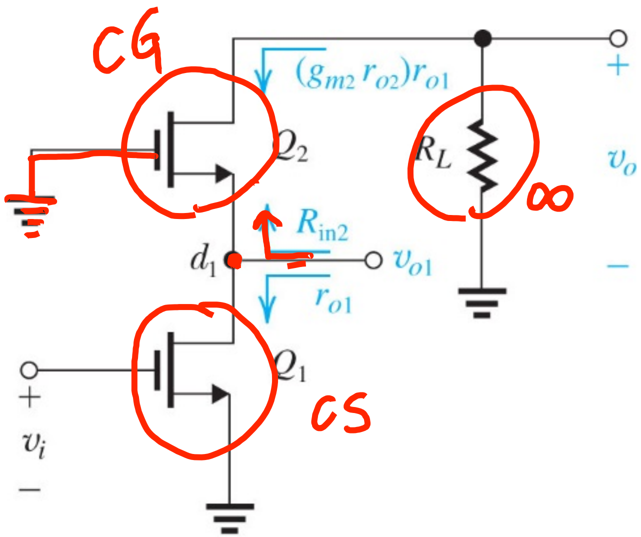
If all transistors are similar :

$$A_v = -\frac{1}{2}(g_m r_o)^2$$

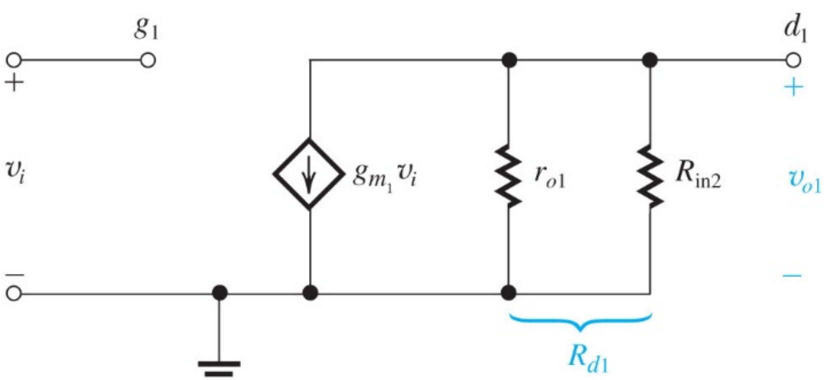
--> High gain !

Thank of Cascode as Multistage Amplifier with CS followed by CG

CS+CG



(a)



First stage: common source

$$A_{v1} = -g_{m1}(r_{o1} \parallel R_{in2}) = -g_{m1} r_{o1}$$

$$R_{in2} = \frac{R_L}{g_{m2} r_{o2}} + \frac{1}{g_{m2}} = \infty$$

Second stage: common gate

$$A_{v2} = g_{m2} r_{o2}$$

$$A_v = A_{v1} A_{v2}$$

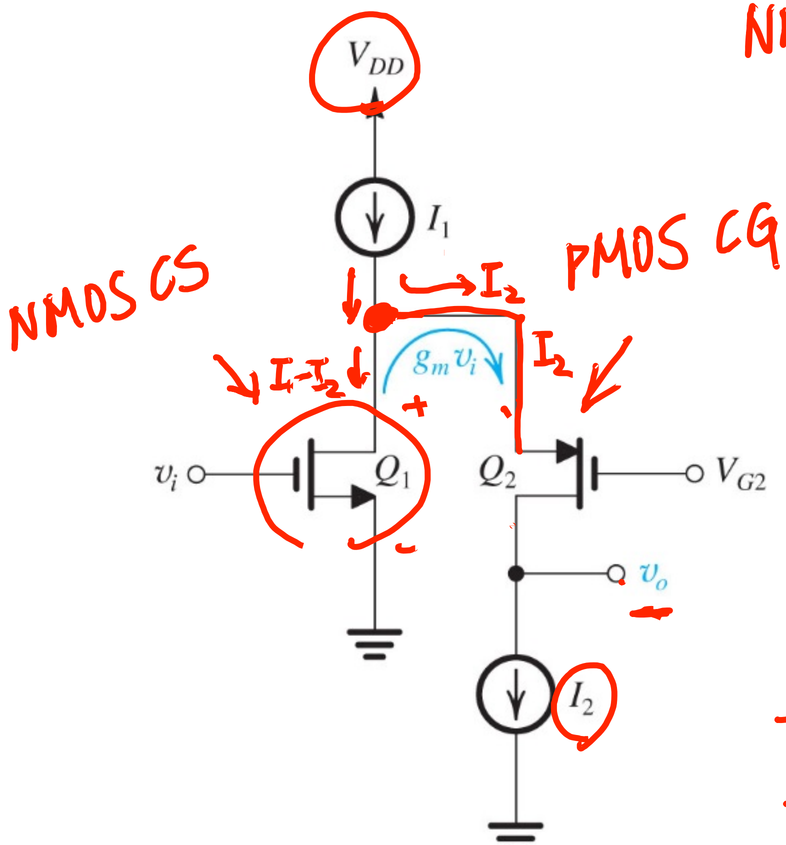
For ideal current source load $R_L = \infty$

$$A_v = (-g_{m1} r_{o1})(g_{m2} r_{o2})$$

Folded Cascode

CS + CG

NMOS PMOS

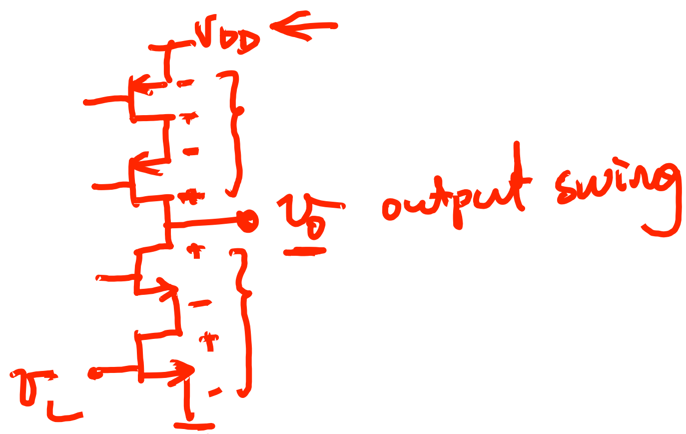


"Folding" the CG stage using PMOS.

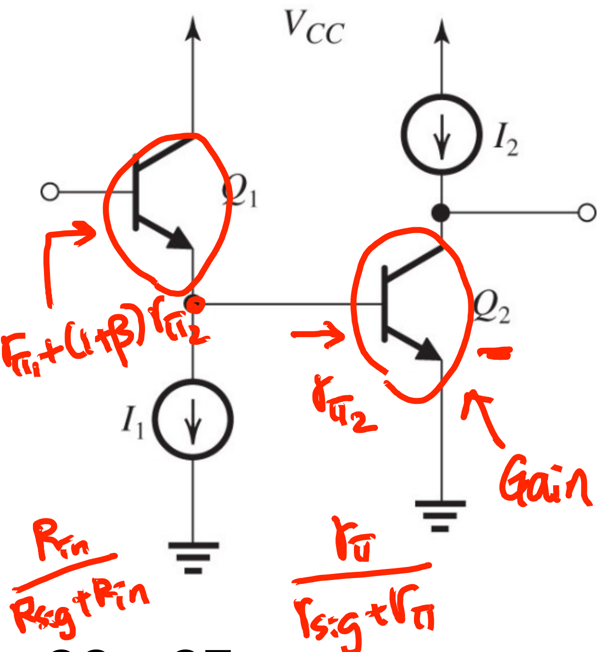
Q_1 is biased with $I_1 - I_2$

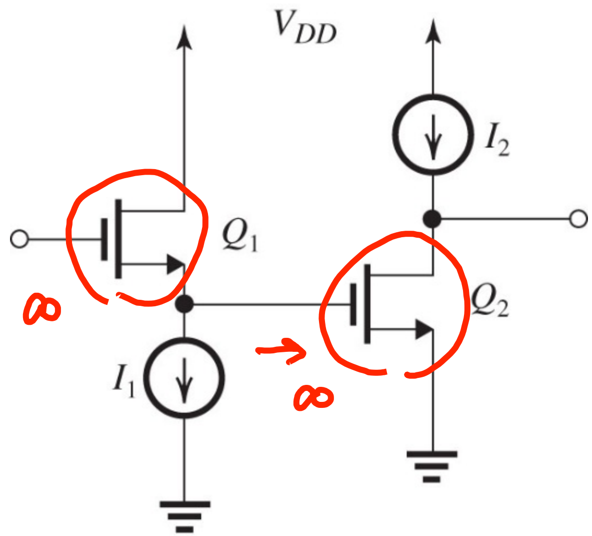
Q_2 is biased with I_2

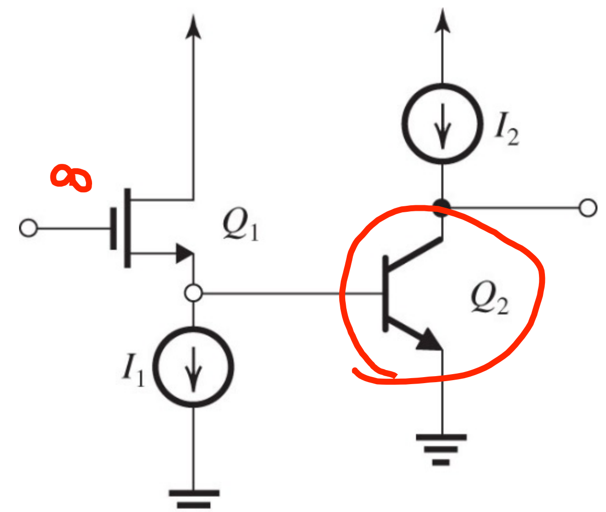
Folded cascode avoids stacking too many transistors vertically, which will be difficult for low power supply voltage V_{DD}



Useful Transistor Pairings





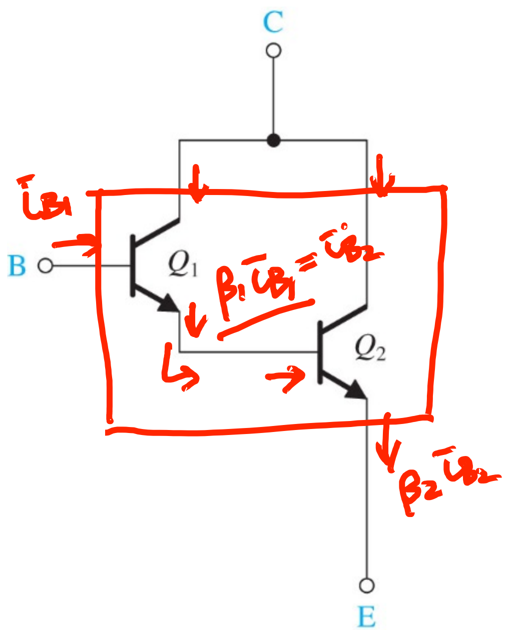


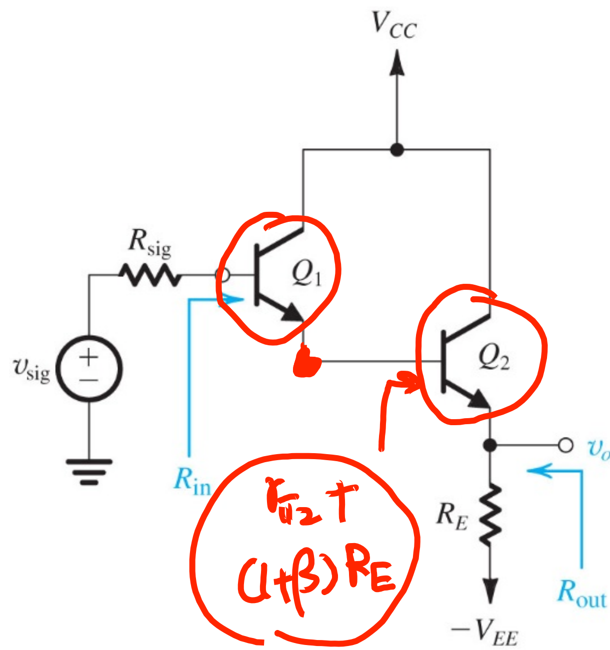
CC + CE
- High input resistance
- Much wider bandwidth than single CE amplifier (To be discussed later)

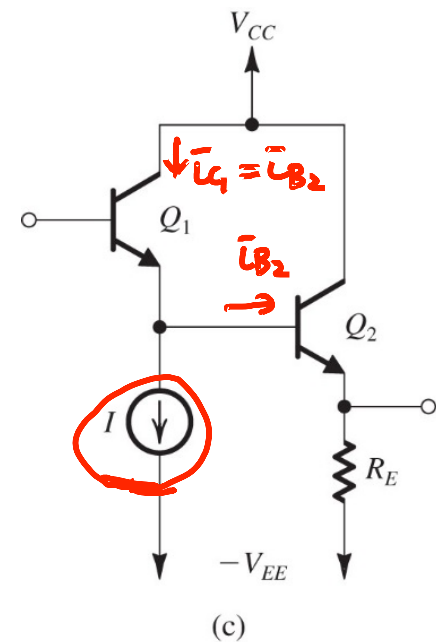
CD + CS
- Main benefit is wider bandwidth than single CE amplifier

CD + CE (BiCMOS technology, or BJT+CMOS)
- Similar to MOS version but BJT has higher g_m

Darlington Pair







Darlington pair:
- **Composite BJT with $\beta = \beta_1\beta_2$**

$$\bar{i}_{C2} = \beta_2 \bar{i}_{B2} = \beta_2\beta_1 \bar{i}_{B2} = \beta \bar{i}_{B2}$$

CC+CC: high performance ~~source~~ emitter follower

$$R_{in} = r_{\pi 1} + (\beta_1+1)\underbrace{\left[r_{\pi 2} + (\beta_2+1)R_E\right]}$$

$$> \beta_1\beta_2 R_E$$

CC+CC: high performance ~~source~~ emitter follower with separate current bias for Q1 → high β_1